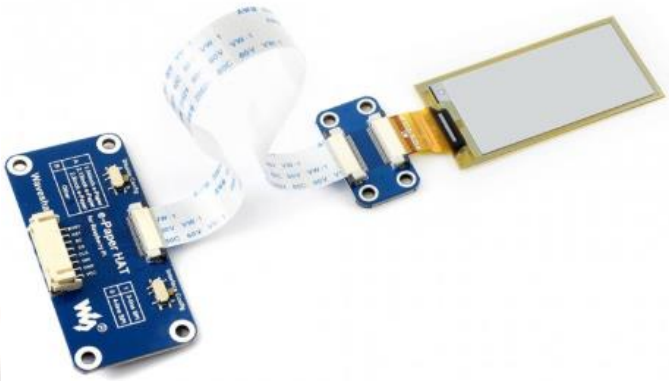
E-PAPER 2.13” HAT D DISPLAY MODULE



Electronic paper is a display technology designed to mimics the appearance of ordinary ink on paper. Unlike a conventional flat panel display, which uses a backlight to illuminate it’s pixels, electronic paper reflects light like ordinary paper. It is capable of holding text and images indefinitely without drawing electricity, while allowing the image to be changed later. To build e-paper, several different technologies exist, some using plastic substrate and electronics, so that display is flexible. E-paper has the potential to be more comfortable to read than conventional display. This is due to the stable image, which does not need to be refreshed constantly, the wider viewing angle, and the fact that it reflects ambient light rather than it’s own light. An e-paper display can be read in direct sunlight without the image appearing to fade.

This is an E-Ink display HAT for Raspberry Pi, 2.13 inch, 212x104 resolution, with embedded controller, communicating via SPI interface, supports partial refresh. Compared with normal e- paper panels, this flexible panel allows bending without being damaged, and it’s thinner and lighter. Combined with the advantages like ultra low power consumption, wide viewing angle, clear display without electricity, it is an ideal choice for applications where curved surface display is required , smart wearable devices, and so on.

This product is an E-paper device adopting the image display technology of Microencapsulated Electrophoretic Display, MED. The initial approach is to create tiny spheres, in which the charged color pigments are suspending in the transparent oil and would move depending on the electronic charge. The E-paper screen display patterns by reflecting the ambient light, so it has no background light requirement. Under sunshine, the E-paper screen still has high visibility with a wide viewing angle of 180 degrees. It is the ideal choice for E-reading.

FEATURES:

- No backlight, keeps displaying last content for a long time even when power down
- Flexible e-Paper, the display section is bendable (Don't bend the FPC section)
- Ultra low power consumption, basically power is only required for refreshing
- Standard Raspberry Pi 40 pin GPIO extension header, supports Raspberry Pi series boards, Jetson Nano
- SPI interface, for connecting with controller boards like Raspberry Pi/Arduino/Nucleo, etc.
- Onboard voltage translator, compatible with 3.3V/5V MCUs
- Comes with development resources and manual (examples for Raspberry Pi/Jetson Nano/Arduino/STM32)

SPECIFICATIONS:

- Operating voltage: 3.3V/5V
- Interface: 3-wire SPI, 4-wire SPI
- Outline dimension: 59.2mm × 29.2mm
- Display size: 23.71mm × 48.55mm
- Dot pitch: 0.229 × 0.228
- Resolution: 212 × 104
- Display color: black, white
- Grey level: 2
- Full refresh time: 2s
- Refresh power: 26.4mW(typ.)
- Standby power: <0.017mW
- Viewing angle: >170°

INTERFACE:

SYMBOL	DESCRIPTION
VCC	Power positive (3.3V power input)
GND	Ground
DIN	SPI MOSI pin
CLK	SPI SCK pin
CS	SPI chip selection, low active
DC	Data/command selection (high for data, low for command
RST	External reset pin (low for reset)
BUSY	Busy status output pin (low for busy)

COMMUNICATION PROTOCOL:

Note: Different from the traditional SPI protocol, the data line from the slave to the master is hidden since the device only has a display requirement.

CS is slave chip select, when CS is low, the chip is enabled.

DC is data/command control pin, when DC = 0, write command, when DC = 1, write data.

SCLK is the SPI communication clock

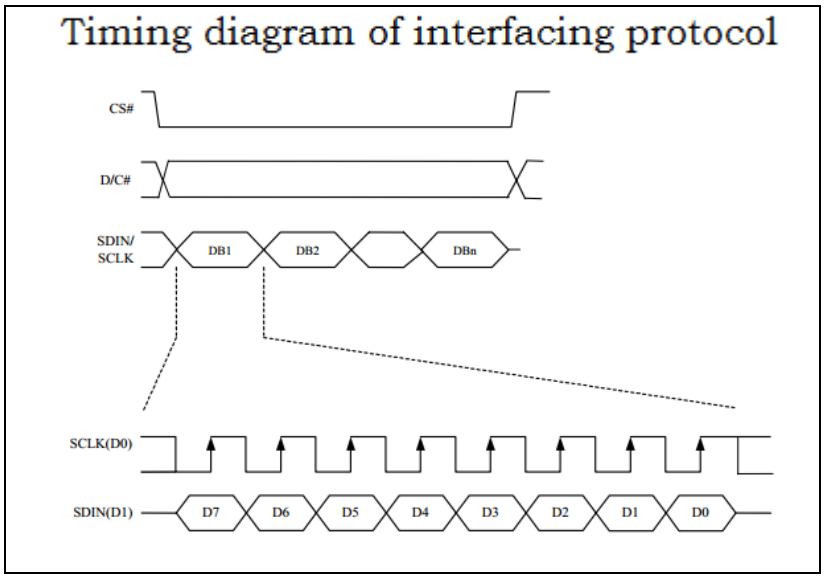
SDIN is the data line from the master to the slave in SPI communication.

SPI communication has data transfer timing, which is combined by CPHA and CPOL.

1. CPOL determines the level of the serial synchronous clock at idle state. When CPOL = 0, the level is Low. However, CPOL has little effect to the transmission.
2. CPHA determines whether data is collected at the first clock edge or at the second clock edge of serial synchronous clock; when CPHL = 0, data is collected at the first clock edge.

There are 4 SPI communication modes. SPI0 is commonly used, in which CPHL = 0, CPOL = 0.

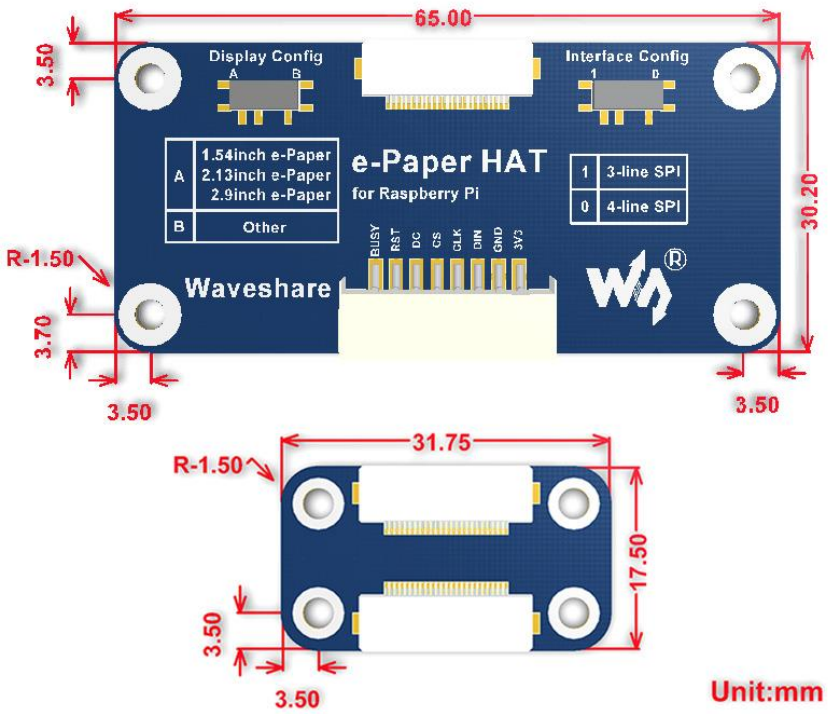
As you can see from the figure above, data transmission starts at the first falling edge of SCLK, and 8 bits of data are transferred in one clock cycle. In here, SPI0 is in used, and data is transferred by bits, MSB first.



PACKAGE INCLUDE:

- 2.13 inch e-Paper HAT(D) x1
- RPi screws pack (2pcs) x 1
- PH2.0 20cm 8Pin x1
- e- Paper Driver HAT x 1

OUTER DIMENSION:



APPLICATIONS:

- Education: Digital school books
- Wristwatches
- E-Books
- Newspaper
- Cell phones
- Status display